01. COVER

CONTENT

Disclaimer:

SchematicS are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

VPC1

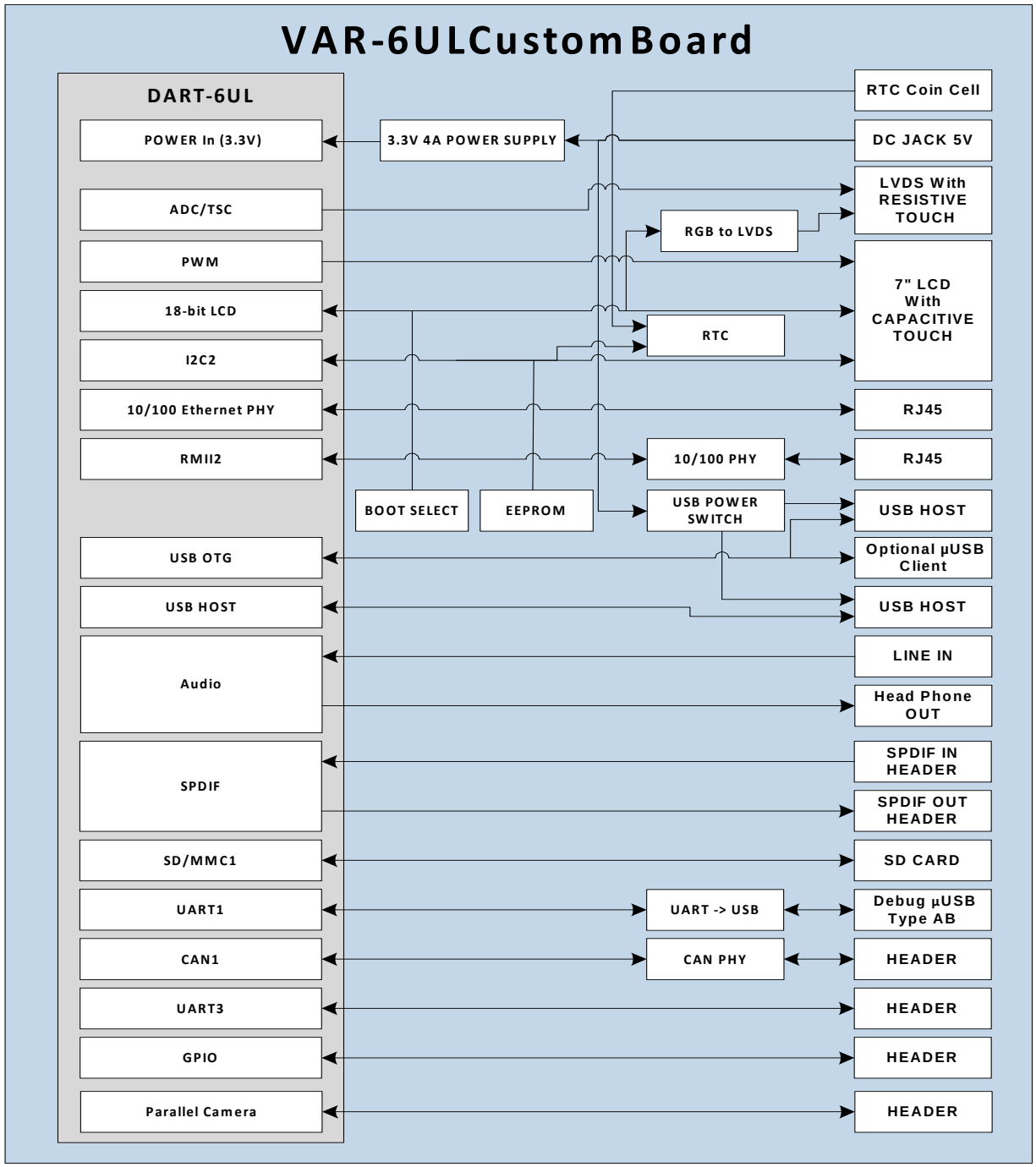
PCB

Revision History

Document	Carrier	Description
1.0	Rev 1.2	Release
1.1	Rev 1.2	SAI1 & SAI2 pin names switched to follow the SOM
1.2	Rev 1.2	CPI Pins added to extension headers
1.3	Rev 1.21	Removed I2C2 pull up resistors Removed not connected boot strap, uSD, Ethernet resistors Added boot strap table
1.4	Rev 1.21	Changed J1.63 pin name
1.5	Rev 1.21A	32khz clock for Wi-Fi module is supplied from iMX6UL processor. R44 not connected, R45 connected
1.6	Rev 1.22	Added filtering on Audio Line In, Headphone lines
1.7	Rev 1.23	R105 pull-down and delay mecahnism added on DEBUG_UART_RTS_B to allow reboot from SD Card using POR button Watchdog signal connected to POR circuitry for proper SW reset
1.8	Rev 1.23	Updated page 3 note 13 Updated page 7 On/Off signal note
1.9	Rev 1.23	Updated page 8 pinmux of pins J1.35, J1.43
2.0	Rev 1.23	J2.77,J2.83 - Added note for SOMs with iMX6UL 'G3' variant
2.1	Rev 1.23	Updated note for UART2 interface
2.2	Rev 1.23A	R107 value changed to strong Pull Up to prevent system reset when entering suspend
2.3	Rev 1.23A	Added note for USB ports

Title: 01. Cover			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Monday, January 29, 2018		Sheet 1 of 9	

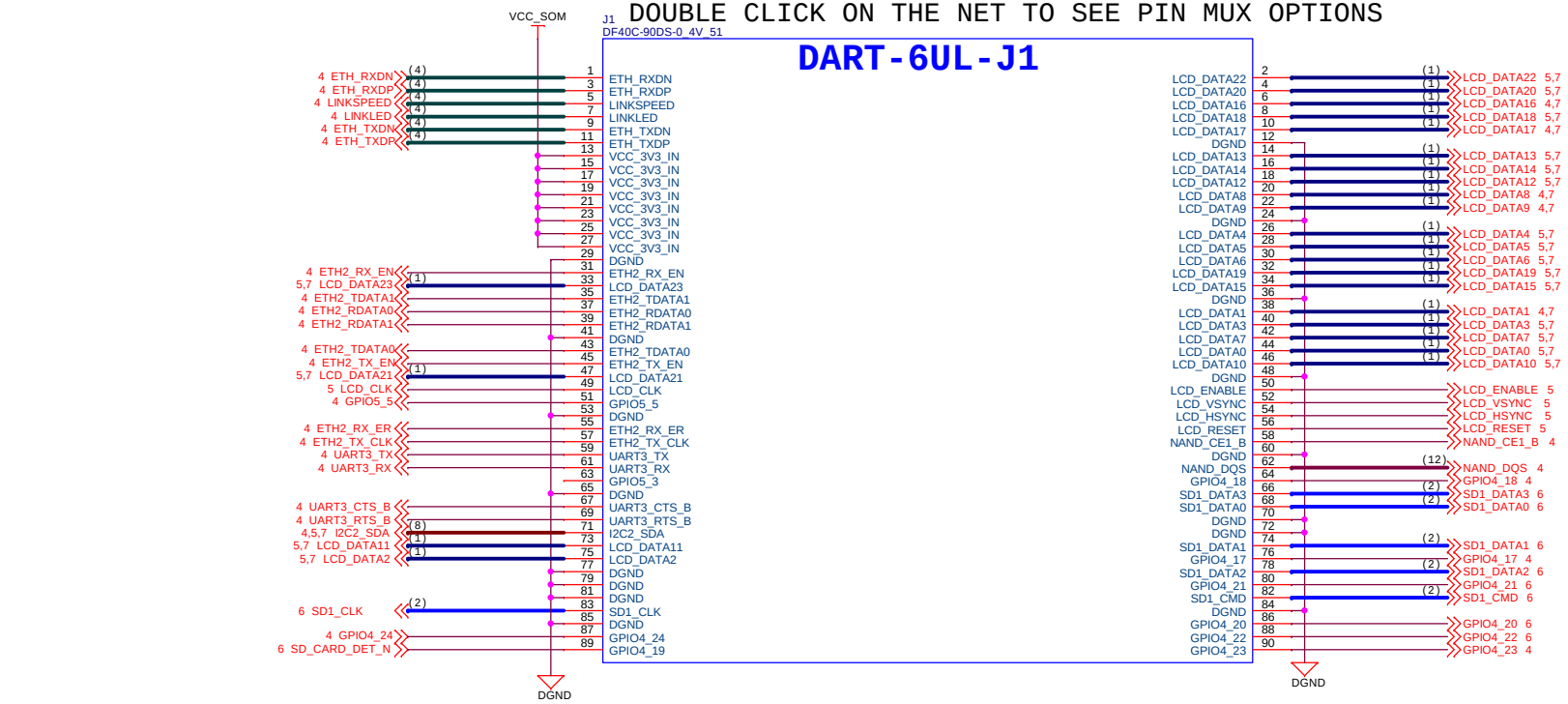
02. Block Diagram

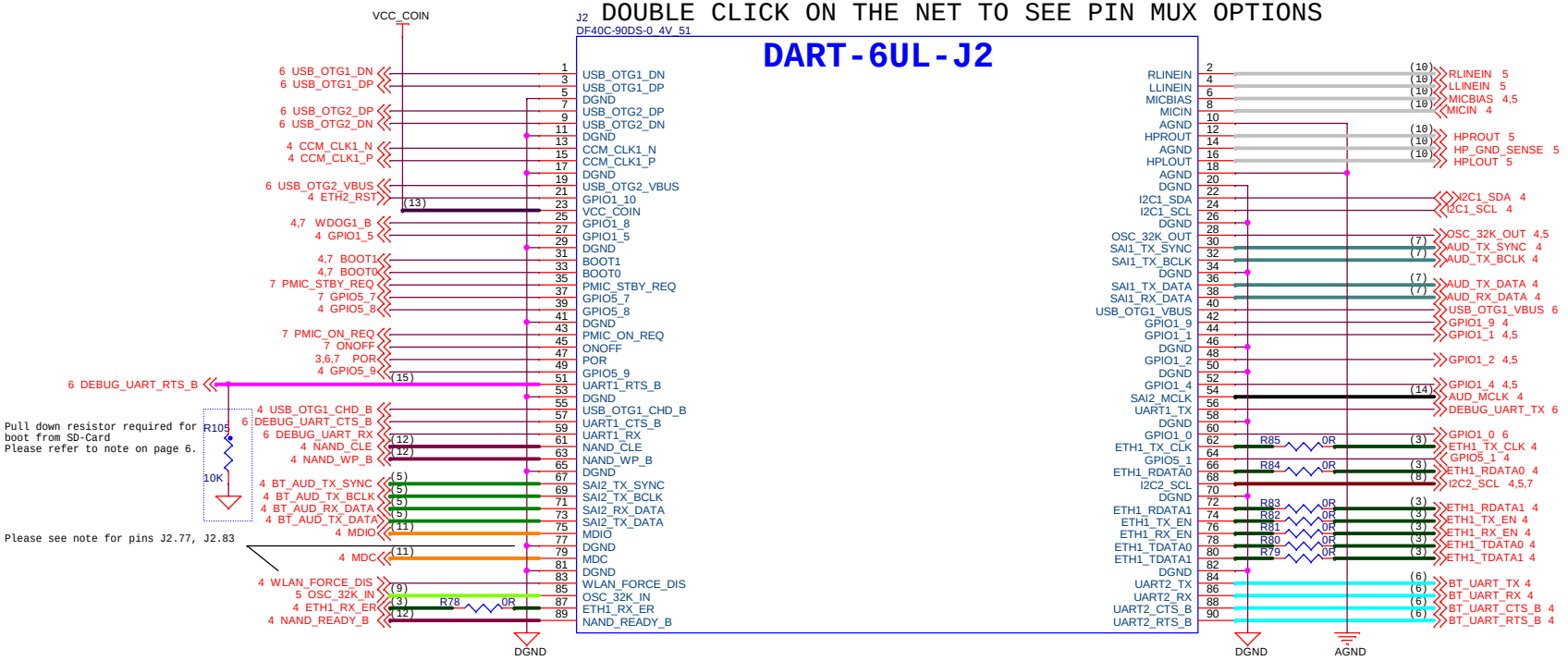


Variscite

Title: 02. Block Diagram			
Size: A3	Document Number:	Project:	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 2 of 9	

03. DART-6UL CONNECTORS





Notes:	Description
(1)	LCD Data Lines are boot strap lines. The should be pulled up/down to select different boot options. Care should be taken if using these lines as inputs to the SOM. Please see the POWER page of this schematics for reference.
(2)	SD1 Interface used internally by the WiFi. The SD can not be used when the WiFi module is enabled. GPIO5_IO6 should be low to use. Other functions beside SD1 can be accessed only on SOMs without WiFi assembled
(3)	ETH1 Interface is used by on SOM PHY. The lines should be not connected when the internal PHY is used. GPIO
(4)	PHY Ethernet interface. Available only on SOMs with Ethernet PHY assembled
(5)	SAI2 Audio interface. Used by Audio Codec or On SOM Bluetooth module to transfer audio. Can be used on SOM without both BT Audio and AUDIO codec assembled
(6)	UART2 interface. Used by On SOM Bluetooth module. DART-6UL: Can be used on SOM without Wi-Fi assembled or BT interface is disabled. DART-6UL-5G: Can be used on SOM without Wi-Fi assmebled or without BT assembled
(7)	SAI1 Interface. Used only by On SOM with both BT AUDIO and Audio codec assembled. The interface can be used on most of the SOMs.
(8)	I2C2 Interface. Used by On SOM Peripherals. The addresses in use by SOM are: 0x1A, 0x50, 0x51. Pin Mode cannot be changed.
(9)	OSC_32K_IN is used On SOM WiFi module. Usuallly this pin is connected to J2.28
(10)	Audio interface. Available only on SOMs with Audio Codec assembled
(11)	MDIO Interface (CPU Balls K17, L16) is used On SOM Ethernet PHY chip. Pin Mode cannot be changed if Ethernet PHY is assembled.
(12)	NAND Interface. Used by On SOM NAND chip. Can be used only in case of eMMC version of the SOM is used.
(13)	iMX6UL SNVS power domain voltage supply input. Must be connected to 3.0 battery or 3.3V power supply.
(14)	Audio Codec Clock signal. Available only on SOMs with Audio Codec not assembled
(15)	Pin is used as SD1_CD_B by Boot ROM, Pull down resistor and delay mecahnism are required. Please refer to USB DEBUG notes on page 6.

Note:

In SOMs assembled with iMX6UL 'G3' variant automatic SD1 routing selection is not available. In such SOMs, controlling SD1 interface routing should be done manually using pins J2.77 and J2.83 as follows:

DART-6UL:

Pin#	SD1 interface routed to J1	SD1 interface routed to WiFi
J2.83	Connect to DGND	Floating
J2.77	Connect to DGND	Connect to DGND

DART-6UL-5G:

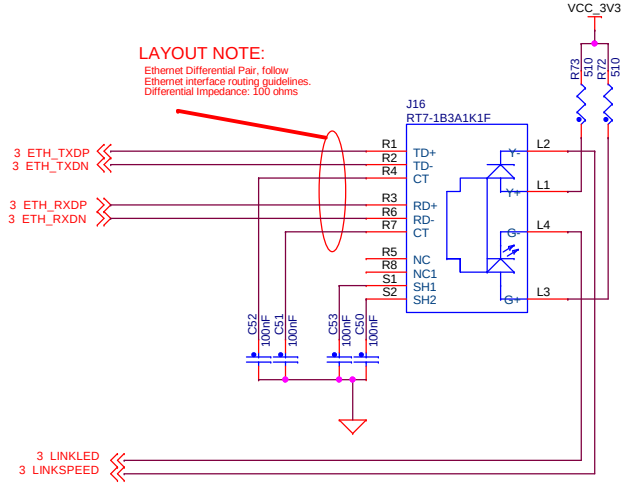
Pin#	SD1 interface routed to J1	SD1 interface routed to WiFi
J2.83	Connect to DGND	Floating
J2.77	Connect to DGND	Connect to 3.3V

Variscite

Title: 03. DART-6UL CONNECTORS			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 3 of 9	

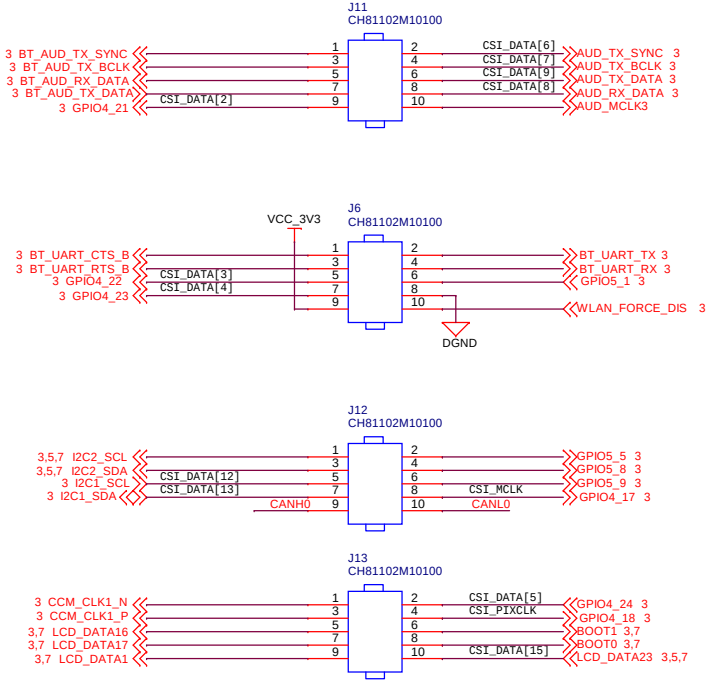
04. ETHERNET, EXTENSION

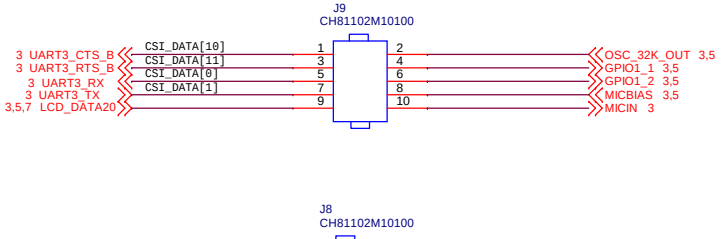
Internal 10/100 Mbps Ethernet

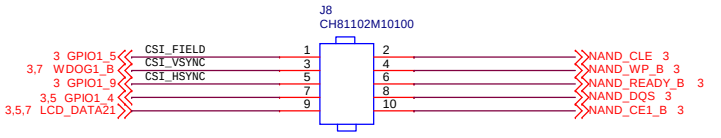


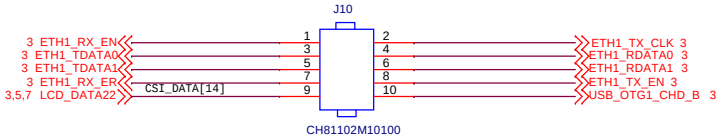
Extension Connectors

Digital Audio

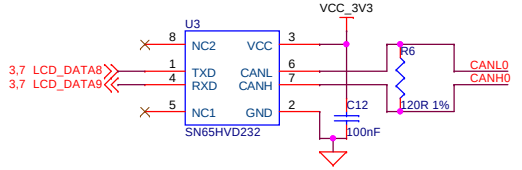




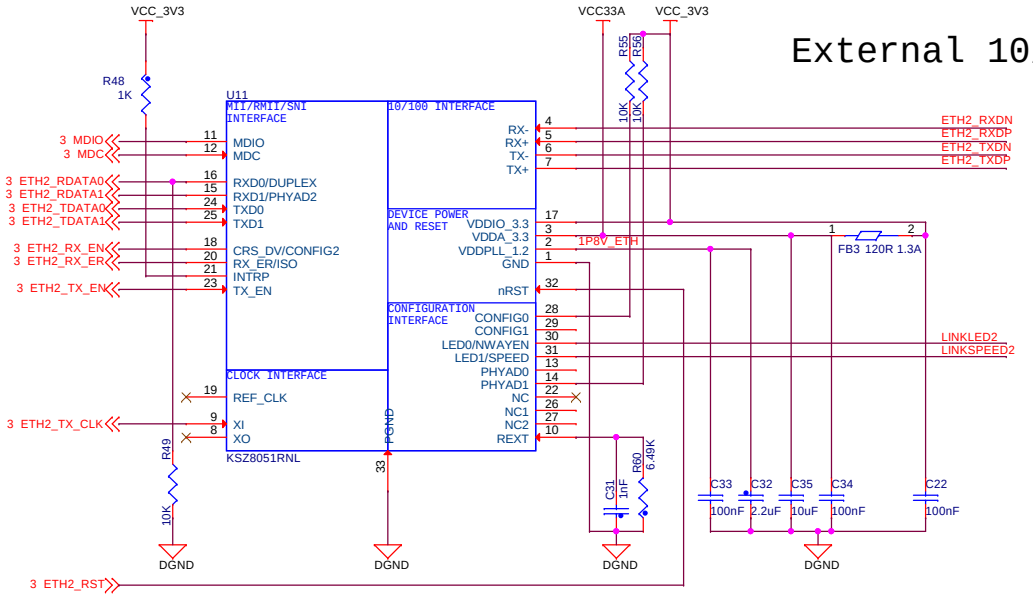


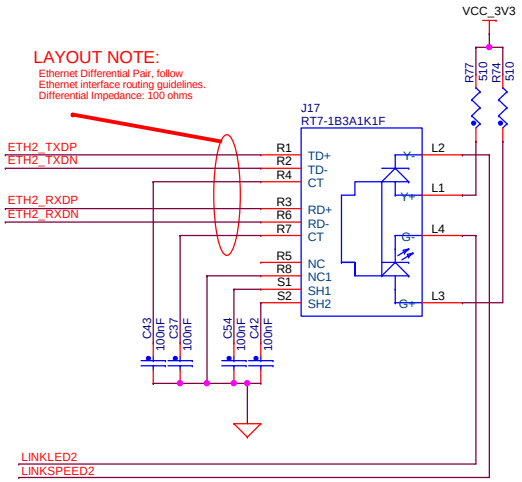


CAN0



External 10/100 Mbps Ethernet



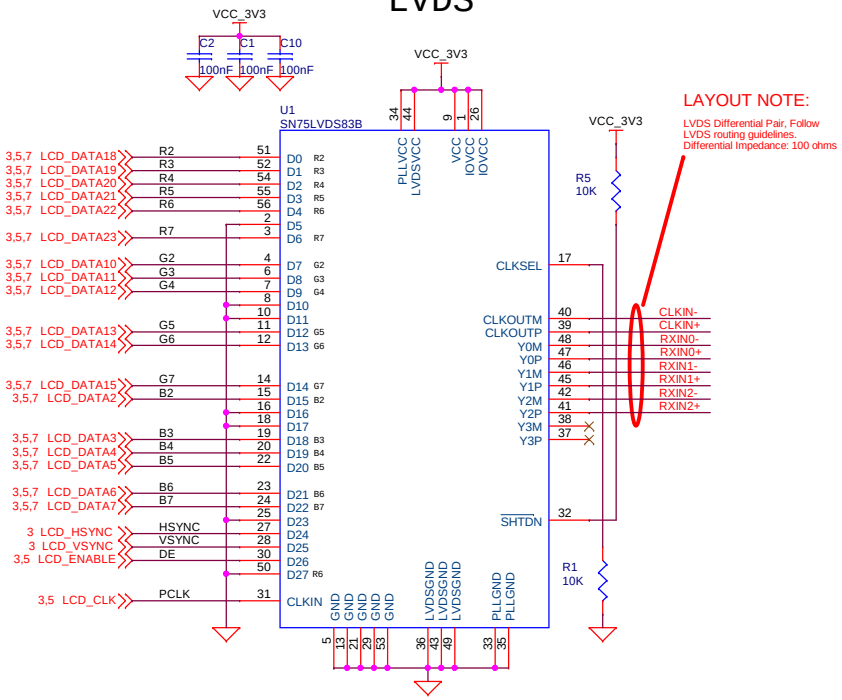


Variscite

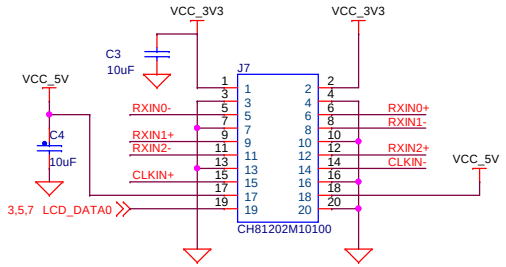
Title: 04. ETHERNET, EXTENSION			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 4 of 9	

05. LCD, AUDIO

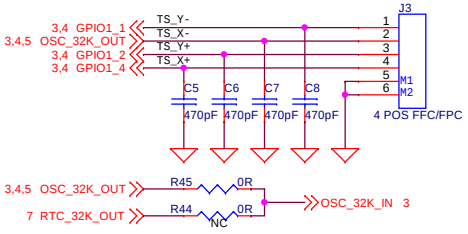
LVDS



LVDS Connector

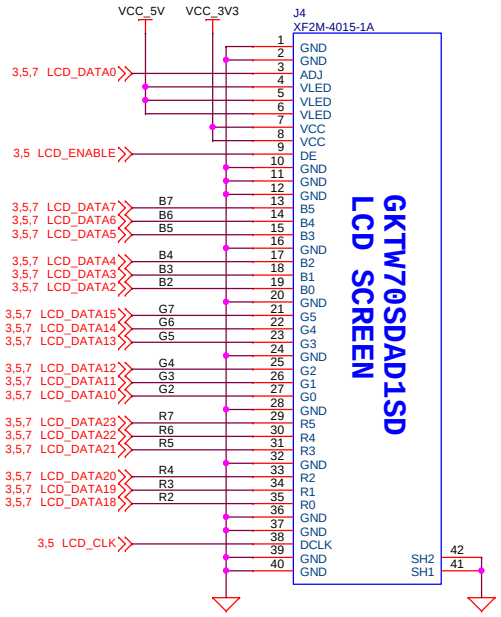


Resistive Touch

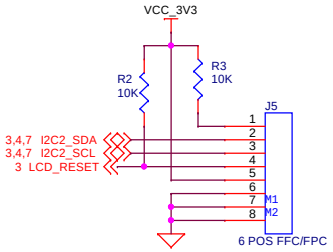


Normally OSC_32K_OUT from MX6UL processor supplies accurate 32Khz for Wi-Fi module.
If this pin is used for resitive touch panel, use alternate 32khz OSC, such as the RTC output one.

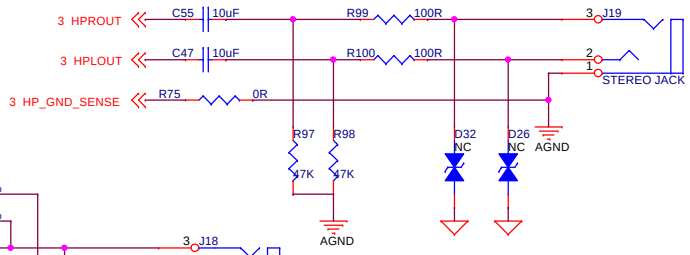
RGB LCD



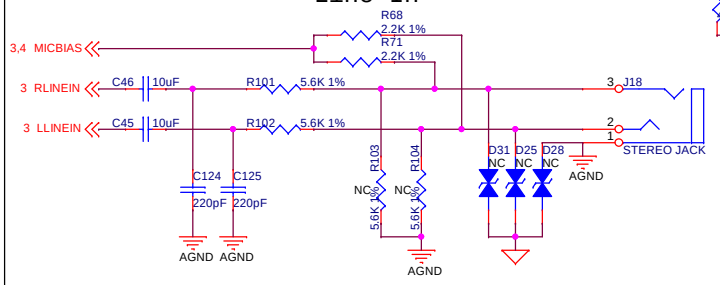
Capacitive touch



Headphones



Line In



Place R68,R71 when connecting Microphone inputs
Place R103,R104 when connecting Line In inputs with 2Vrms levels

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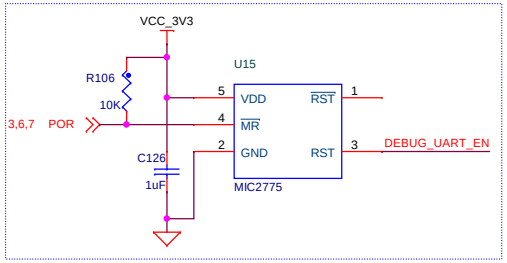
Title: 05. LCD, AUDIO			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 5 of 9	

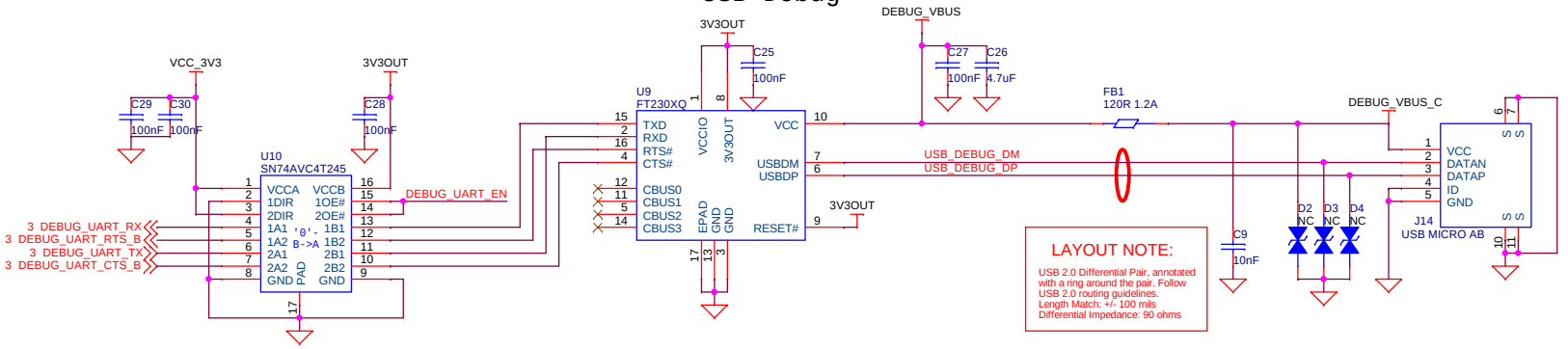
06. SD, USB

Note:
Pull down resistor and delay circuitry is added on
DEBUG_UART_RTS_B to allow reboot from SD Card using POR signal,
since DEBUG_UART_RTS_B is used as SD1_CD_B by Boot ROM.

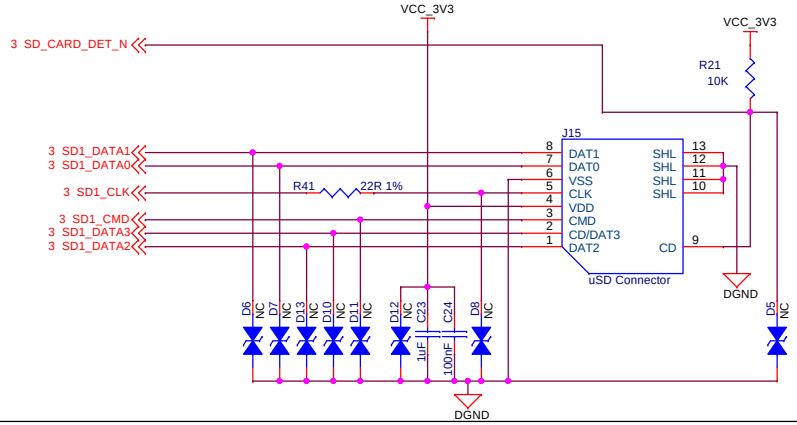
In case DEBUG_UART_RTS_B signal is not required,
the delay mechanism is redundant and can be depopulated.
DEBUG_UART_RTS_B however should be always
pulled down to ground using a 10K resistor to simulate SD Card detect.



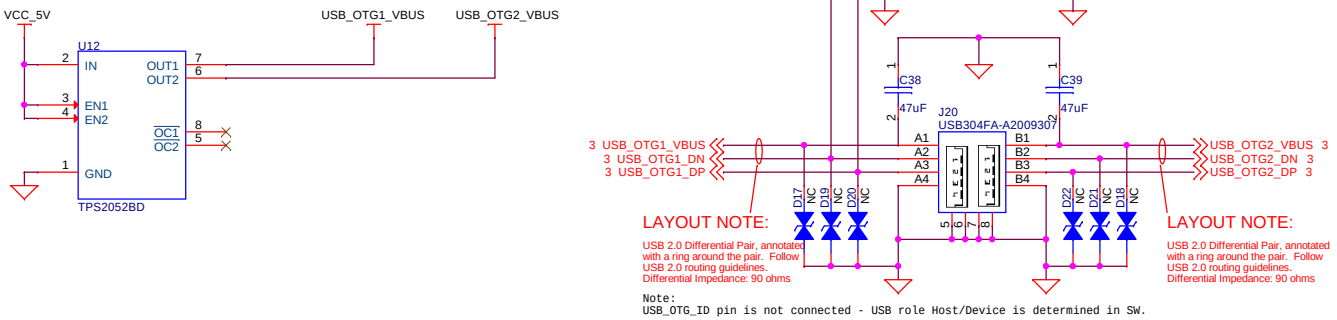
USB Debug



uSD CARD

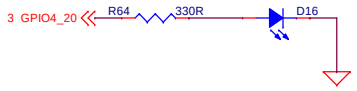


USB

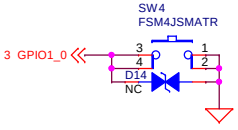


Note:
USB_OTG_ID pin is not connected - USB role Host/Device is determined in SW.

User LED



User Buttom

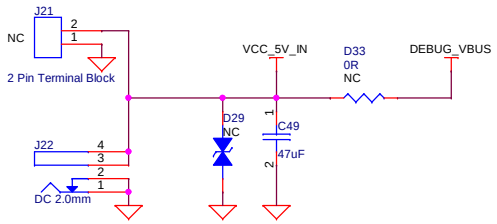


Variscite

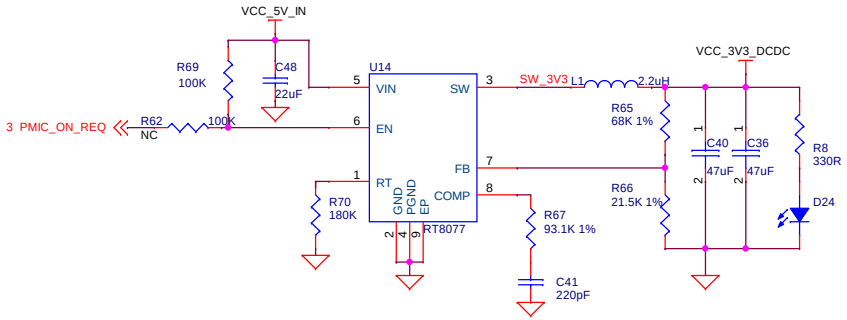
Title: 06. SD, USB			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Monday, January 29, 2018		Sheet 6 of 9	

07. POWER

Power in 5VDC



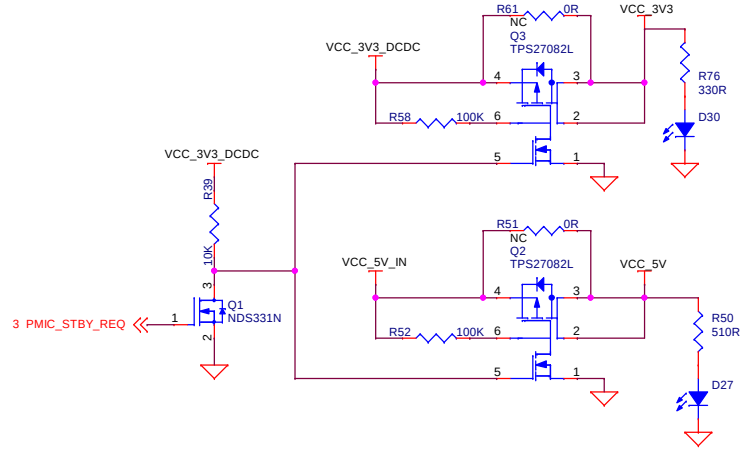
MAIN 3.3V POWER SUPPLY



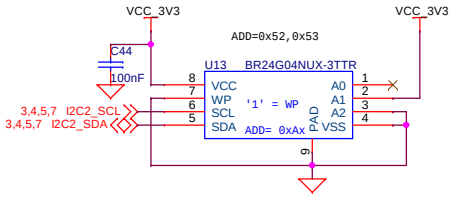
The On/Off button is connected to the On/Off signal of the iMX6UL CPU.
Long press (approx 7sec) on this button will reset the system and reboot.

Alternatively, the button can be used to power Off the module by long press.
Then, when in Off state, power On the module again by short press.
In order to achieve this: assemble R62, R46; disassemble R47 and R69; insert the coin cell battery into JBT1.

3.3V Base

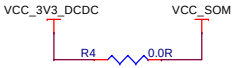


Board ID

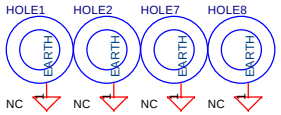


ON/OFF Button

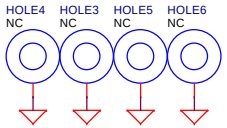
SOM Power



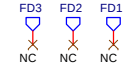
4X Chassis Holes



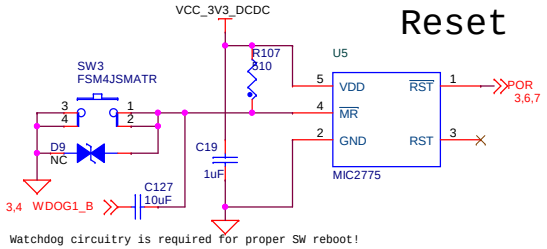
4X SOM CONN HOLES



Fiducial



Reset

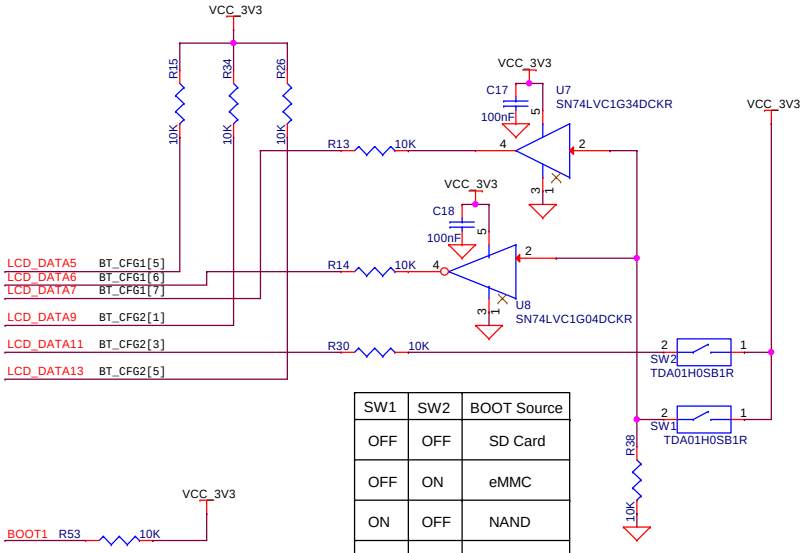


Watchdog circuitry is required for proper SW reboot!

Boot strap

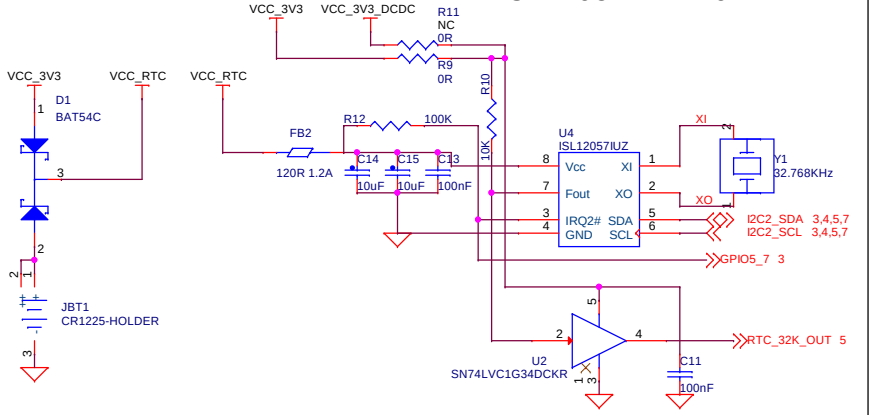
		NAND	eMMC	SD Card
3,5 LCD_DATA0	BT_CFG1[0]	0	0	0
3,4 LCD_DATA1	BT_CFG1[1]	0	0	0
3,5 LCD_DATA2	BT_CFG1[2]	0	0	0
3,5 LCD_DATA3	BT_CFG1[3]	0	0	0
3,5 LCD_DATA4	BT_CFG1[4]	0	0	0
3,5 LCD_DATA5	BT_CFG1[5]	1	1	1
3,5 LCD_DATA6	BT_CFG1[6]	0	1	1
3,5 LCD_DATA7	BT_CFG1[7]	1	0	0
3,4 LCD_DATA8	BT_CFG2[0]	0	0	0
3,4 LCD_DATA9	BT_CFG2[1]	1	1	1
3,5 LCD_DATA10	BT_CFG2[2]	0	0	0
3,5 LCD_DATA11	BT_CFG2[3]	x	1	0
3,5 LCD_DATA12	BT_CFG2[4]	0	0	0
3,5 LCD_DATA13	BT_CFG2[5]	1	1	1
3,5 LCD_DATA14	BT_CFG2[6]	0	0	0
3,5 LCD_DATA15	BT_CFG2[7]	0	0	0
3,4 LCD_DATA16	BT_CFG4[0]	0	0	0
3,4 LCD_DATA17	BT_CFG4[1]	0	0	0
3,5 LCD_DATA18	BT_CFG4[2]	0	0	0
3,5 LCD_DATA19	BT_CFG4[3]	0	0	0
3,5 LCD_DATA20	BT_CFG4[4]	0	0	0
3,5 LCD_DATA21	BT_CFG4[5]	0	0	0
3,5 LCD_DATA22	BT_CFG4[6]	0	0	0
3,5 LCD_DATA23	BT_CFG4[7]	0	0	0
3,4 BOOT0	BOOT_MODE[0]	0	0	0
3,4 BOOT1	BOOT_MODE[1]	1	1	1

Note:
0 – Pull down or floating.
1 – Pull up of 10K or stronger.
X – Don't care.



SW1	SW2	BOOT Source
OFF	OFF	SD Card
OFF	ON	eMMC
ON	OFF	NAND
ON	ON	NAND

ISL12057 - RTC



Variscite

Title: 07. POWER			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 7 of 9	

08. PIN MUX J1

	PIN#	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
3,5,7 LCD_DATA22	J1.02	LCD_DATA[22]	MQS_RIGHT	ECSPI1_MOSI	CSI_DATA[14]	WEIM_DATA[14]	GPIO3_IO[27]	BT_CFG[30]	TPSMP_HDATA[0]	USDHC2_DATA2
3,5,7 LCD_DATA20	J1.04	LCD_DATA[20]	UART8_TX	ECSPI1_SCLK	CSI_DATA[12]	WEIM_DATA[12]	GPIO3_IO[25]	BT_CFG[28]	TPSMP_HTRANS[0]	USDHC2_DATA0
3,4,7 LCD_DATA16	J1.06	LCD_DATA[16]	UART7_TX	CA7_PLATFORM_TRACE_CLK	CSI_DATA[1]	WEIM_DATA[8]	GPIO3_IO[21]	BT_CFG[24]	SIM_M_HSIZE[2]	USDHC2_DATA6
3,5,7 LCD_DATA18	J1.08	LCD_DATA[18]	PWM5_OUT	CA7_PLATFORM_EVENTO	CSI_DATA[10]	WEIM_DATA[10]	GPIO3_IO[23]	BT_CFG[26]	TPSMP_CLK	USDHC2_CMD
3,4,7 LCD_DATA17	J1.10	LCD_DATA[17]	UART7_RX	CA7_PLATFORM_TRACE_CTL	CSI_DATA[0]	WEIM_DATA[9]	GPIO3_IO[22]	BT_CFG[25]	SIM_M_HWRITE	USDHC2_DATA7
3,5,7 LCD_DATA13	J1.14	LCD_DATA[13]	SAI3_TX_BCLK	CA7_PLATFORM_TRACE[13]	CSI_DATA[21]	WEIM_DATA[5]	GPIO3_IO[18]	BT_CFG[13]	SIM_M_HRESP	USDHC2_RESET
3,5,7 LCD_DATA14	J1.16	LCD_DATA[14]	SAI3_RX_DATA	CA7_PLATFORM_TRACE[14]	CSI_DATA[22]	WEIM_DATA[6]	GPIO3_IO[19]	BT_CFG[14]	SIM_M_HSIZE[0]	USDHC2_DATA4
3,5,7 LCD_DATA12	J1.18	LCD_DATA[12]	SAI3_TX_SYNC	CA7_PLATFORM_TRACE[12]	CSI_DATA[20]	WEIM_DATA[4]	GPIO3_IO[17]	BT_CFG[12]	SIM_M_HREADYOUT	ECSPI1_RDY
3,4,7 LCD_DATA8	J1.20	LCD_DATA[8]	SPDIF_IN	CA7_PLATFORM_TRACE[8]	CSI_DATA[16]	WEIM_DATA[0]	GPIO3_IO[13]	BT_CFG[8]	SIM_M_HPROT[0]	CAN1_TX
3,4,7 LCD_DATA9	J1.22	LCD_DATA[9]	SAI3_MCLK	CA7_PLATFORM_TRACE[9]	CSI_DATA[17]	WEIM_DATA[1]	GPIO3_IO[14]	BT_CFG[9]	SIM_M_HPROT[1]	CAN1_RX
3,5,7 LCD_DATA4	J1.26	LCD_DATA[4]	UART8_CTS	CA7_PLATFORM_TRACE[4]	ENET2_1588_EVENT2_IN	SPDIF_SR_CLK	GPIO3_IO[9]	BT_CFG[4]	SIM_M_HBURST[0]	SAI1_TX_DATA
3,5,7 LCD_DATA5	J1.28	LCD_DATA[5]	UART8_RTS	CA7_PLATFORM_TRACE[5]	ENET2_1588_EVENT2_OUT	SPDIF_OUT	GPIO3_IO[10]	BT_CFG[5]	SIM_M_HBURST[1]	ECSPI1_SS1
3,5,7 LCD_DATA6	J1.30	LCD_DATA[6]	UART7_CTS	CA7_PLATFORM_TRACE[6]	ENET2_1588_EVENT3_IN	SPDIF_LOCK	GPIO3_IO[11]	BT_CFG[6]	SIM_M_HBURST[2]	ECSPI1_SS2
3,4 ETH2_RX_EN	J1.31	ENET2_RX_EN	UART7_TX	SIM1_PORT0_RST	I2C4_SCL	WEIM_ADDR[26]	GPIO2_IO[10]	KPP_ROW[5]	<ALT7>	ANATOP_ENET_REF_CLK_25M
3,5,7 LCD_DATA19	J1.32	LCD_DATA[19]	PWM6_OUT	GLOBAL_WDOG	CSI_DATA[11]	WEIM_DATA[11]	GPIO3_IO[24]	BT_CFG[27]	TPSMP_HDATA_DIR	USDHC2_CLK
3,5,7 LCD_DATA23	J1.33	LCD_DATA[23]	MQS_LEFT	ECSPI1_MISO	CSI_DATA[15]	WEIM_DATA[15]	GPIO3_IO[28]	BT_CFG[31]	TPSMP_HDATA[1]	USDHC2_DATA3
3,5,7 LCD_DATA15	J1.34	LCD_DATA[15]	SAI3_TX_DATA	CA7_PLATFORM_TRACE[15]	CSI_DATA[23]	WEIM_DATA[7]	GPIO3_IO[20]	BT_CFG[15]	SIM_M_HSIZE[1]	USDHC2_DATA5
3,4 ETH2_TDATA1	J1.35	ENET2_TDATA[1]	UART8_TX	SIM2_PORT0_TRXD	ECSPI4_SCLK	WEIM_EB_B[3]	GPIO2_IO[12]	KPP_ROW[6]	<ALT7>	USB_OTG2_PWR
3,4 ETH2_RDATA0	J1.37	ENET2_RDATA[0]	UART6_TX	SIM1_PORT0_TRXD	I2C3_SCL	ENET1_MDIO	GPIO2_IO[8]	KPP_ROW[4]	<ALT7>	USB_OTG1_PWR
3,4,7 LCD_DATA1	J1.38	LCD_DATA[1]	PWM2_OUT	CA7_PLATFORM_TRACE[1]	ENET1_1588_EVENT2_OUT	I2C3_SCL	GPIO3_IO[6]	BT_CFG[1]	SIM_M_HADDR[29]	SAI1_TX_SYNC
3,4 ETH2_RDATA1	J1.39	ENET2_RDATA[1]	UART6_RX	SIM1_PORT0_CLK	I2C3_SDA	ENET1_MDC	GPIO2_IO[9]	KPP_COL[4]	<ALT7>	USB_OTG1_OC
3,5,7 LCD_DATA3	J1.40	LCD_DATA[3]	PWM4_OUT	CA7_PLATFORM_TRACE[3]	ENET1_1588_EVENT3_OUT	I2C4_SCL	GPIO3_IO[8]	BT_CFG[3]	SIM_M_HADDR[31]	SAI1_RX_DATA
3,5,7 LCD_DATA7	J1.42	LCD_DATA[7]	UART7_RTS	CA7_PLATFORM_TRACE[7]	ENET2_1588_EVENT3_OUT	SPDIF_EXT_CLK	GPIO3_IO[12]	BT_CFG[7]	SIM_M_HMASTLOCK	ECSPI1_SS3
3,4 ETH2_TDATA0	J1.43	ENET2_TDATA[0]	UART7_RX	SIM1_PORT0_SVEN	I2C4_SDA	WEIM_EB_B[2]	GPIO2_IO[11]	KPP_COL[5]	<ALT7>	ANATOP_24M_OUT
3,5,7 LCD_DATA0	J1.44	LCD_DATA[0]	PWM1_OUT	CA7_PLATFORM_TRACE[0]	ENET1_1588_EVENT2_IN	I2C3_SDA	GPIO3_IO[5]	BT_CFG[0]	SIM_M_HADDR[28]	SAI1_MCLK
3,4 ETH2_TX_EN	J1.45	ENET2_TX_EN	UART8_RX	SIM2_PORT0_CLK	ECSPI4_MOSI	WEIM_ACLK_FREERUN	GPIO2_IO[13]	KPP_COL[6]	SIM_M_HADDR[20]	USB_OTG2_OC
3,5,7 LCD_DATA10	J1.46	LCD_DATA[10]	SAI3_RX_SYNC	CA7_PLATFORM_TRACE[10]	CSI_DATA[18]	WEIM_DATA[2]	GPIO3_IO[15]	BT_CFG[10]	SIM_M_HPROT[2]	CAN2_TX
3,5,7 LCD_DATA21	J1.47	LCD_DATA[21]	UART8_RX	ECSPI1_SS0	CSI_DATA[13]	WEIM_DATA[13]	GPIO3_IO[26]	BT_CFG[29]	TPSMP_HTRANS[1]	USDHC2_DATA1
3,5 LCD_CLK	J1.49	LCD_CLK	LCD_WR_RWN	UART4_TX	SAI3_MCLK	WEIM_CS2	GPIO3_IO[0]	OCOTP_CTRL_WRAPPER_FUSE_LATCHED	SIM_M_HADDR[23]	WDOG1_WDOG_RST_DEB
3,5 LCD_ENABLE	J1.50	LCD_ENABLE	LCD_RD_E	UART4_RX	SAI3_TX_SYNC	WEIM_CS3	GPIO3_IO[1]	ANATOP_TESTI[0]	SIM_M_HADDR[24]	ECSPI2_RDY
3,4 GPIO5_5	J1.51*	TAMPER[5]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[5]	<ALT6>	<ALT7>	<ALT8>
3,5 LCD_VSYNC	J1.52	LCD_VSYNC	LCD_BUSY	UART4_RTS	SAI3_RX_DATA	WDOG2_WDOG	GPIO3_IO[3]	ANATOP_TESTI[2]	SIM_M_HADDR[26]	ECSPI2_SS2
3,5 LCD_HSYNC	J1.54	LCD_HSYNC	LCD_RS	UART4_CTS	SAI3_TX_BCLK	WDOG3_WDOG_RST_DEB	GPIO3_IO[2]	ANATOP_TESTI[1]	SIM_M_HADDR[25]	ECSPI2_SS1
3,4 ETH2_RX_ER	J1.55	ENET2_RX_ER	UART8_RTS	SIM2_PORT0_SVEN	ECSPI4_SS0	WEIM_ADDR[25]	GPIO2_IO[15]	KPP_COL[7]	<ALT7>	GLOBAL_WDOG
3,5 LCD_RESET	J1.56	LCD_RESET	LCD_CS	CA7_PLATFORM_EVENTI	SAI3_TX_DATA	GLOBAL_WDOG	GPIO3_IO[4]	ANATOP_TESTI[3]	SIM_M_HADDR[27]	ECSPI2_SS3
3,4 ETH2_TX_CLK	J1.57	ENET2_TX_CLK	UART8_CTS	SIM2_PORT0_RST	ECSPI4_MISO	ANATOP_ENET_REF_CLK2	GPIO2_IO[14]	KPP_ROW[7]	SIM_M_HADDR[21]	ANATOP_OTG2_ID
3,4 NAND_CE1_B	J1.58	RAWNAND_CE1	USDHC1_DATA6	QSPIA_DATA[2]	ECSPI3_MOSI	WEIM_ADDR[18]	GPIO4_IO[14]	ANATOP_TESTO[14]	TPSMP_HDATA[16]	UART3_CTS
3,4 UART3_TX	J1.59	UART3_TX	ENET2_RDATA[2]	SIM1_PORT0_PD	CSI_DATA[1]	UART2_CTS	GPIO1_IO[24]	ANATOP_USBPHY1_TSTI_TX_DP	JTAG_ACT	ANATOP_OTG1_ID
3,4 UART3_RX	J1.61	UART3_RX	ENET2_RDATA[3]	SIM2_PORT0_PD	CSI_DATA[0]	UART2_RTS	GPIO1_IO[25]	ANATOP_USBPHY1_TSTI_TX_EN	SIM_M_HADDR[0]	EPIT1_OUT
3,4 NAND_DQS	J1.62	RAWNAND_DQS	CSI_FIELD	QSPIA_SS0	PWM5_OUT	WEIM_WAIT	GPIO4_IO[16]	SDMA_EXT_EVENT[1]	TPSMP_HDATA[17]	SPDIF_EXT_CLK
3,4 GPIO4_18	J1.64	CSI_PIXCLK	USDHC2_WP	RAWNAND_CE3	I2C1_SCL	WEIM_OE	GPIO4_IO[18]	SNVS_HP_WRAPPER_VIO_5	TPSMP_HDATA[21]	UART6_RX
3,6 SD1_DATA3	J1.66*	USDHC1_DATA3	GPT2_CAPTURE2	SAI2_TX_DATA	CAN2_RX	WEIM_ADDR[24]	GPIO2_IO[21]	CCM_CLKO2	OBSERVE_MUX_OUT[4]	ANATOP_OTG2_ID
3,4 UART3_CTS_B	J1.67	UART3_CTS	ENET2_RX_CLK	CAN1_TX	CSI_DATA[10]	ENET1_1588_EVENT1_IN	GPIO1_IO[26]	ANATOP_USBPHY1_TSTI_TX_HIZ	SIM_M_HADDR[1]	EPIT2_OUT
3,6 SD1_DATA0	J1.68*	USDHC1_DATA0	GPT2_COMPARE3	SAI2_TX_SYNC	CAN1_TX	WEIM_ADDR[21]	GPIO2_IO[18]	CCM_OUT1	OBSERVE_MUX_OUT[1]	ANATOP_OTG1_ID
3,4 UART3_RTS_B	J1.69	UART3_RTS	ENET2_TX_ER	CAN1_RX	CSI_DATA[11]	ENET1_1588_EVENT1_OUT	GPIO1_IO[27]	ANATOP_USBPHY2_TSTO_RX_HS_RXD	SIM_M_HADDR[2]	WDOG1_WDOG
3,4,5,7 I2C2_SDA	J1.71*	UART5_RX	ENET2_COL	I2C2_SDA	CSI_DATA[15]	CSU_CSU_INT_DEB	GPIO1_IO[31]	ANATOP_USBPHY2_TSTO_RX_DISCON_DET	SIM_M_HADDR[6]	ECSPI2_MISO
3,5,7 LCD_DATA11	J1.73	LCD_DATA[11]	SAI3_RX_BCLK	CA7_PLATFORM_TRACE[11]	CSI_DATA[19]	WEIM_DATA[3]	GPIO3_IO[16]	BT_CFG[11]	SIM_M_HPROT[3]	CAN2_RX
3,6 SD1_DATA1	J1.74*	USDHC1_DATA1	GPT2_CLK	SAI2_TX_BCLK	CAN1_RX	WEIM_ADDR[22]	GPIO2_IO[19]	CCM_OUT2	OBSERVE_MUX_OUT[2]	USB_OTG2_PWR
3,5,7 LCD_DATA2	J1.75	LCD_DATA[2]	PWM3_OUT	CA7_PLATFORM_TRACE[2]	ENET1_1588_EVENT3_IN	I2C4_SDA	GPIO3_IO[7]	BT_CFG[2]	SIM_M_HADDR[30]	SAI1_TX_BCLK
3,4 GPIO4_17	J1.76	CSI_MCLK	USDHC2_CD	RAWNAND_CE2	I2C1_SDA	WEIM_CS0	GPIO4_IO[17]	SNVS_HP_WRAPPER_VIO_5_CTL	TPSMP_HDATA[20]	UART6_TX
3,6 SD1_DATA2	J1.78*	USDHC1_DATA2	GPT2_CAPTURE1	SAI2_RX_DATA	CAN2_TX	WEIM_ADDR[23]	GPIO2_IO[20]	CCM_CLKO1	OBSERVE_MUX_OUT[3]	USB_OTG2_OC
3,6 GPIO4_21	J1.80	CSI_DATA[2]	USDHC2_DATA0	SIM1_PORT1_RST	ECSPI2_SCLK	WEIM_AD[0]	GPIO4_IO[21]	INT_BOOT	TPSMP_HDATA[24]	UART5_TX
3,6 SD1_CMD	J1.82*	USDHC1_CMD	GPT2_COMPARE1	SAI2_RX_SYNC	SPDIF_OUT	WEIM_ADDR[19]	GPIO2_IO[16]	SDMA_EXT_EVENT[0]	TPSMP_HDATA[18]	USB_OTG1_PWR
3,6 SD1_CLK	J1.83*	USDHC1_CLK	GPT2_COMPARE2	SAI2_MCLK	SPDIF_IN	WEIM_ADDR[20]	GPIO2_IO[17]	CCM_OUT0	OBSERVE_MUX_OUT[0]	USB_OTG1_OC
3,6 GPIO4_20	J1.86	CSI_HSYNC	USDHC2_CMD	SIM1_PORT1_PD	I2C2_SCL	WEIM_LBA	GPIO4_IO[20]	PWM8_OUT	TPSMP_HDATA[23]	UART6_CTS
3,4 GPIO4_24	J1.87	CSI_DATA[5]	USDHC2_DATA3	SIM2_PORT1_PD	ECSPI2_MISO	WEIM_AD[3]	GPIO4_IO[24]	SAI1_RX_BCLK	<ALT7>	UART5_CTS
3,4 GPIO4_22	J1.88	CSI_DATA[3]	USDHC2_DATA1	SIM1_PORT1_SVEN	ECSPI2_SS0	WEIM_AD[1]	GPIO4_IO[22]	SAI1_MCLK	TPSMP_HDATA[25]	UART5_RX
3,6 SD_CARD_DET_N	J1.89	CSI_VSYNC	USDHC2_CLK	SIM1_PORT1_CLK	I2C2_SDA	WEIM_RW	GPIO4_IO[19]	PWM7_OUT	TPSMP_HDATA[22]	UART6_RTS
3,4 GPIO4_23	J1.90	CSI_DATA[4]	USDHC2_DATA2	SIM1_PORT1_TRXD	ECSPI2_MOSI	WEIM_AD[2]	GPIO4_IO[23]	SAI1_RX_SYNC	TPSMP_HDATA[26]	UART5_RTS

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Title	08. PIN MUX J1		
Size A3	Document Number	Project	Rev 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 8 of 9	

09. PIN MUX J2

	PIN#	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
3,4 ETH2_RST	J2.21	MOD	GPT2_CLK	SPDIF_OUT	ANATOP_ENET_REF_CLK_25M	CCM_PMIC_RDY	GPIO1_IO[10]	SDMA_EXT_EVENT[0]	<ALT7>	<ALT8>
3,4 I2C1_SDA	J2.22	UART4_RX	ENET2_TDATA[3]	I2C1_SDA	CSI_DATA[13]	CSU_CSU_ALARM_AUT[1]	GPIO1_IO[29]	ANATOP_USBPHY2_TSTO_PLL_CLK20DIV	SIM_M_HADDR[4]	ECSPI2_SS0
3,4 I2C1_SCL	J2.24	UART4_TX	ENET2_TDATA[2]	I2C1_SCL	CSI_DATA[12]	CSU_CSU_ALARM_AUT[2]	GPIO1_IO[28]	ANATOP_USBPHY1_TSTO_PLL_CLK20DIV	SIM_M_HADDR[3]	ECSPI2_SCLK
3,4 WDOG1_B	J2.25	PWM1_OUT	WDOG1_WDOG	SPDIF_OUT	CSI_VSYNC	USDHC2_VSELECT	GPIO1_IO[8]	CCM_PMIC_RDY	ECSPI2_TESTER_TRIGGER	UART5_RTS
3,4 GPIO1_5	J2.27	ANATOP_ENET_REF_CLK2	PWM4_OUT	ANATOP_OTG2_ID	CSI_FIELD	USDHC1_VSELECT	GPIO1_IO[5]	ENET2_1588_EVENT0_OUT	CCM_PLL3_BYP	UART5_RX
3,4,5 OSC_32K_OUT	J2.28*	I2C1_SDA	GPT1_COMPARE3	USB_OTG2_OC	OSC32K_32K_OUT	USDHC1_CD	GPIO1_IO[3]	CCM_DI0_EXT_CLK	TESTER_ACK	UART1_RX
3,4 AUD_TX_SYNC	J2.30*	CSI_DATA[6]	USDHC2_DATA4	SIM2_PORT1_CLK	ECSPI1_SCLK	WEIM_AD[4]	GPIO4_IO[25]	SAI1_TX_SYNC	TPSMP_HDATA[28]	USDHC1_WP
3,4,7 BOOT1	J2.31	BOOT_MODE[1]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[11]	<ALT6>	<ALT7>	<ALT8>
3,4 AUD_TX_BCLK	J2.32*	CSI_DATA[7]	USDHC2_DATA5	SIM2_PORT1_RST	ECSPI1_SS0	WEIM_AD[5]	GPIO4_IO[26]	SAI1_TX_BCLK	TPSMP_HDATA[29]	USDHC1_CD
3,4,7 BOOT0	J2.33	BOOT_MODE[0]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[10]	<ALT6>	<ALT7>	<ALT8>
3,4 AUD_TX_DATA	J2.36*	CSI_DATA[9]	USDHC2_DATA7	SIM2_PORT1_TRXD	ECSPI1_MISO	WEIM_AD[7]	GPIO4_IO[28]	SAI1_TX_DATA	TPSMP_HDATA[31]	USDHC1_VSELECT
3,7 GPIO5_7	J2.37	TAMPER[7]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[7]	<ALT6>	<ALT7>	<ALT8>
3,4 AUD_RX_DATA	J2.38*	CSI_DATA[8]	USDHC2_DATA6	SIM2_PORT1_SVEN	ECSPI1_MOSI	WEIM_AD[6]	GPIO4_IO[27]	SAI1_RX_DATA	TPSMP_HDATA[30]	USDHC1_RESET
3,4 GPIO5_8	J2.39	TAMPER[8]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[8]	<ALT6>	<ALT7>	<ALT8>
3,4 GPIO1_9	J2.42	PWM2_OUT	GLOBAL_WDOG	SPDIF_IN	CSI_HSYNC	USDHC2_RESET	GPIO1_IO[9]	USDHC1_RESET	ECSPI3_TESTER_TRIGGER	UART5_CTS
3,4,5 GPIO1_1	J2.44	I2C2_SDA	GPT1_COMPARE1	USB_OTG1_OC	ANATOP_ENET_REF_CLK2	MQS_LEFT	GPIO1_IO[1]	ENET1_1588_EVENT0_OUT	EARLY_RESET	WDOG1_WDOG
3,4,5 GPIO1_2	J2.48	I2C1_SCL	GPT1_COMPARE2	USB_OTG2_PWR	ANATOP_ENET_REF_CLK_25M	USDHC1_WP	GPIO1_IO[2]	SDMA_EXT_EVENT[0]	ANY_PU_RESET	UART1_TX
3,4 GPIO5_9	J2.49	TAMPER[9]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[9]	<ALT6>	<ALT7>	<ALT8>
3,6 DEBUG_UART_RTS_B	J2.51	UART1_RTS	ENET1_TX_ER	USDHC1_CD	CSI_DATA[5]	ENET2_1588_EVENT1_OUT	GPIO1_IO[19]	ANATOP_USBPHY1_TSTO_RX_SQUELCH	QSPI_TESTER_TRIGGER	USDHC2_CD
3,4,5 GPIO1_4	J2.52	ANATOP_ENET_REF_CLK1	PWM3_OUT	USB_OTG1_PWR	ANATOP_24M_OUT	USDHC1_RESET	GPIO1_IO[4]	ENET2_1588_EVENT0_IN	CCM_PLL2_BYP	UART5_TX
3,4 AUD_MCLK	J2.54*	TMS	GPT2_CAPTURE1	SAI2_MCLK	CCM_CLKO1	CCM_WAIT	GPIO1_IO[11]	SDMA_EXT_EVENT[1]	<ALT7>	EPIT1_OUT
3,6 DEBUG_UART_TX	J2.56	UART1_TX	ENET1_RDATA[2]	I2C3_SCL	CSI_DATA[2]	GPT1_COMPARE1	GPIO1_IO[16]	ANATOP_USBPHY1_TSTI_TX_LS_MODE	ECSPI4_TESTER_TRIGGER	SPDIF_OUT
3,6 DEBUG_UART_CTS_B	J2.57	UART1_CTS	ENET1_RX_CLK	USDHC1_WP	CSI_DATA[4]	ENET2_1588_EVENT1_IN	GPIO1_IO[18]	ANATOP_USBPHY1_TSTI_TX_DN	USDHC2_TESTER_TRIGGER	USDHC2_WP
3,6 DEBUG_UART_RX	J2.59	UART1_RX	ENET1_RDATA[3]	I2C3_SDA	CSI_DATA[3]	GPT1_CLK	GPIO1_IO[17]	ANATOP_USBPHY1_TSTI_TX_HS_MODE	USDHC1_TESTER_TRIGGER	SPDIF_IN
3,6 GPIO1_0	J2.60	I2C2_SCL	GPT1_CAPTURE1	ANATOP_OTG1_ID	ANATOP_ENET_REF_CLK1	MQS_RIGHT	GPIO1_IO[0]	ENET1_1588_EVENT0_IN	SYSTEM_RESET	WDOG3_WDOG
3,4 NAND_CLE	J2.61*	RAWNAND_CLE	USDHC1_DATA7	QSPIA_DATA[3]	ECSPI3_MISO	WEIM_ADDR[16]	GPIO4_IO[15]	ANATOP_TESTO[15]	TPSMP_HDATA[19]	UART3_RTS
3,4 ETH1_TX_CLK	J2.62*	ENET1_TX_CLK	UART7_CTS	PWM7_OUT	CSI_DATA[22]	ANATOP_ENET_REF_CLK1	GPIO2_IO[6]	KPP_ROW[3]	SIM_M_HADDR[13]	GPT1_CLK
3,4 NAND_WP_B	J2.63*	RAWNAND_WP	USDHC1_RESET	QSPIA_SCLK	PWM4_OUT	WEIM_BCLK	GPIO4_IO[11]	ANATOP_TESTO[11]	TPSMP_HDATA[13]	ECSPI3_RDY
3,4 GPIO5_1	J2.64	TAMPER[1]	<ALT1>	<ALT2>	<ALT3>	<ALT4>	GPIO5_IO[1]	<ALT6>	<ALT7>	<ALT8>
3,4 ETH1_RDATA0	J2.66*	ENET1_RDATA[0]	UART4_RTS	PWM1_OUT	CSI_DATA[16]	CAN1_TX	GPIO2_IO[0]	KPP_ROW[0]	SIM_M_HADDR[7]	USDHC1_LCTL
3,4 BT_AUD_TX_SYNC	J2.67*	TDO	GPT2_CAPTURE2	SAI2_TX_SYNC	CCM_CLKO2	CCM_STOP	GPIO1_IO[12]	MQS_RIGHT	<ALT7>	EPIT2_OUT
3,4,5,7 I2C2_SCL	J2.68*	UART5_TX	ENET2_CRS	I2C2_SCL	CSI_DATA[14]	CSU_CSU_ALARM_AUT[0]	GPIO1_IO[30]	ANATOP_USBPHY2_TSTO_RX_SQUELCH	SIM_M_HADDR[5]	ECSPI2_MOSI
3,4 BT_AUD_TX_BCLK	J2.69*	TDI	GPT2_COMPARE1	SAI2_TX_BCLK	CCM_OUT0	PWM6_OUT	GPIO1_IO[13]	MQS_LEFT	<ALT7>	SIM1_POWER_FAIL
3,4 BT_AUD_RX_DATA	J2.71*	TCK	GPT2_COMPARE2	SAI2_RX_DATA	CCM_OUT1	PWM7_OUT	GPIO1_IO[14]	OSC32K_32K_OUT	<ALT7>	SIM2_POWER_FAIL
3,4 ETH1_RDATA1	J2.72*	ENET1_RDATA[1]	UART4_CTS	PWM2_OUT	CSI_DATA[17]	CAN1_RX	GPIO2_IO[1]	KPP_COL[0]	SIM_M_HADDR[8]	USDHC2_LCTL
3,4 BT_AUD_TX_DATA	J2.73*	TRSTB	GPT2_COMPARE3	SAI2_TX_DATA	CCM_OUT2	PWM8_OUT	GPIO1_IO[15]	ANATOP_24M_OUT	<ALT7>	CAAM_WRAPPER_RNG_OSC_OBS
3,4 ETH1_TX_EN	J2.74*	ENET1_TX_EN	UART6_RTS	PWM6_OUT	CSI_DATA[21]	ENET2_MDC	GPIO2_IO[5]	KPP_COL[2]	SIM_M_HADDR[12]	WDOG2_WDOG_RST_DEB
3,4 MDIO	J2.75*	ENET1_MDIO	ENET2_MDIO	USB_OTG_PWR_WAKE	CSI_MCLK	USDHC2_WP	GPIO1_IO[6]	CCM_WAIT	CCM_REF_EN	UART1_CTS
3,4 ETH1_RX_EN	J2.76*	ENET1_RX_EN	UART5_RTS	OSC32K_32K_OUT	CSI_DATA[18]	CAN2_TX	GPIO2_IO[2]	KPP_ROW[1]	SIM_M_HADDR[9]	USDHC1_VSELECT
3,4 ETH1_TDATA0	J2.78*	ENET1_TDATA[0]	UART5_CTS	ANATOP_24M_OUT	CSI_DATA[19]	CAN2_RX	GPIO2_IO[3]	KPP_COL[1]	SIM_M_HADDR[10]	USDHC2_VSELECT
3,4 MDC	J2.79*	ENET1_MDC	ENET2_MDC	USB_OTG_HOST_MODE	CSI_PIXCLK	USDHC2_CD	GPIO1_IO[7]	CCM_STOP	ECSPI1_TESTER_TRIGGER	UART1_RTS
3,4 ETH1_TDATA1	J2.80*	ENET1_TDATA[1]	UART6_CTS	PWM5_OUT	CSI_DATA[20]	ENET2_MDIO	GPIO2_IO[4]	KPP_ROW[2]	SIM_M_HADDR[11]	WDOG1_WDOG_RST_DEB
3,4 BT_UART_TX	J2.84*	UART2_TX	ENET1_TDATA[2]	I2C4_SCL	CSI_DATA[6]	GPT1_CAPTURE1	GPIO1_IO[20]	ANATOP_USBPHY1_TSTO_RX_DISCON_DET	RAWNAND_TESTER_TRIGGER	ECSPI3_SS0
3,4 BT_UART_RX	J2.86*	UART2_RX	ENET1_TDATA[3]	I2C4_SDA	CSI_DATA[7]	GPT1_CAPTURE2	GPIO1_IO[21]	ANATOP_USBPHY1_TSTO_RX_HS_RXD	DONE	ECSPI3_SCLK
3,4 ETH1_RX_ER	J2.87*	ENET1_RX_ER	UART7_RTS	PWM8_OUT	CSI_DATA[23]	WEIM_CRE	GPIO2_IO[7]	KPP_COL[3]	SIM_M_HADDR[14]	GPT1_CAPTURE2
3,4 BT_UART_CTS_B	J2.88*	UART2_CTS	ENET1_CRS	CAN2_TX	CSI_DATA[8]	GPT1_COMPARE2	GPIO1_IO[22]	ANATOP_USBPHY2_TSTO_RX_FS_RXD	DE	ECSPI3_MOSI
3,4 NAND_READY_B	J2.89*	RAWNAND_READY	USDHC1_DATA4	QSPIA_DATA[0]	ECSPI3_SS0	WEIM_CS1	GPIO4_IO[12]	ANATOP_TESTO[12]	TPSMP_HDATA[14]	UART3_TX
3,4 BT_UART_RTS_B	J2.90*	UART2_RTS	ENET1_COL	CAN2_RX	CSI_DATA[9]	GPT1_COMPARE3	GPIO1_IO[23]	ANATOP_USBPHY1_TSTO_RX_FS_RXD	FAIL	ECSPI3_MISO

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Title: 09. PIN MUX J2			
Size: A3	Document Number	Project	Rev: 1.23A
Designer: Leonid S.		Approved By:	
Date: Wednesday, July 26, 2017		Sheet 9 of 9	